## REMARKS

Claims 1, 5, 14 and 17 have been amended to improve form, claims 10-13, 15 and 16 have been canceled without prejudice or disclaimer and new claims 21-22 have been added. Claims 1-9, 14 and 17-22 are now pending in this application.

Claims 1-3, 5, 7, 8, 14-16, 18 and 20 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Fried et al. (U.S. Patent Publication No. 2003/0178670; hereinafter Fried). The rejection is respectfully traversed.

Claim 1 recites a memory device that includes a first gate and a second gate. Claim 1, as amended, recites that the first and second gates are electrically isolated from each other. A similar feature was recited in original claim 16. The Office Action does not particularly address this feature. In any event, Fried does not disclose this feature.

For example, Fried discloses that control gate 120 is a global gate connecting multiple devices across the chip (Fried – page 3 at paragraph 34). As illustrated in Fig. 8 of Fried, control gate 120 may be formed on either side of the floating gates 115. The portions of control gate 120 located on either side of floating gates 115 are electrically connected via the portion of control gate 120 that is located over fin structure 100/102. Therefore, Fried does not disclose first and second gates that are disposed on opposite side of fin 100/102 that are electrically isolated from each other, as required by amended claim 1.

Further, Fried cannot be fairly construed to suggest this feature. For example, Fried explicitly discloses that control gate 120 is a global gate that connects multiple devices across the chip (Fried – page 3 at paragraph 34). Fried, therefore, actually teaches away from the use of first and second gates that are electrically isolated from each other.

The applicants note that Figs. 12 and 13 of Fried illustrate views in which fin stack 105 appears to electrically isolate each side of control gate 120. Fig. 12 of Fried, however, is a cross-sectional view of Fig. 11 taken along line 12-12 of Fig. 11 (Fried – page 4, paragraph 45). Fig. 13 is apparently a similar view taken along line 12-12 of Fig. 11 that illustrates source and drain regions 103a-d in more detail. Therefore, these figures of Fried refer back to Fig. 11, which clearly shows that control gate 120 is electrically connected on both sides of fin structure 105.

For at least these reasons, Fried does not disclose or suggest each of the features of amended claim 1. Accordingly, withdrawal of the rejection and allowance of claim 1 are respectfully requested.

Claims 2, 3, 5, 7 and 8 are dependent on claim 1 and are believed to be allowable for at least the reasons claim 1 is allowable. In addition, these claims recite additional features not disclosed or suggested by Fried.

For example, claim 2 recites a source region and a drain region formed on the insulating layer and disposed adjacent a respective first and second end of the fin structure. The Office Action states that Fried discloses these features and points to source/drain regions 103 of Fried for support (Office Action – page 3). The applicants respectfully disagree.

Fried discloses forming source and drain regions 103a-d in the vertical sides of fin stack 105 (Fried – page 4, paragraphs 39 and 46, see Figs. 11-13). Fried, therefore, does not disclose that the source region and drain regions 103 are disposed adjacent a respective first and second end of the fin structure, as required by claim 2.

For at least this additional reason, withdrawal of the rejection and allowance of claim 2 are respectfully requested.

Claim 5 recites that the first and second gates are associated with corresponding memory cells that are programmed independently of each other. The Office Action states that Fried discloses that the gate formed over the floating gate may be a single gate or multiple gates and therefore, would be programmed independently and points to page 2, paragraph 20 for support (Office Action – page 3). The applicants respectfully disagree.

Fried at paragraph 20 discloses that single or double FinFET structures may be provided with the FinFET structures covered by single or double spacer-like floating gates and covered by single or multiple control gates. The applicants note that Fried does not illustrate how the multiple control gates would be formed and all the illustrated embodiments of Fried show control gate 120 associated with the single or double floating gates being an electrically continuous gate structure (See, for example, Figs. 8, 10 and 11). Further, Fried refers to control gate 120 as being a "global gate" connecting multiple devices (Fried – page 3, paragraph 34). The applicants, therefore, assert that without any additional description of how the multiple control gate structure is configured in Fried or how the device operates, the mere statement that multiple control gates can be formed over the double floating gates cannot be fairly construed to disclose that first and second gates in Fried are associated with corresponding memory cells that are programmed independently of each other, as required by claim 5.

For at least this additional reason, withdrawal of the rejection and allowance of claim 5 are respectfully requested.

Claim 14, as amended, recites features similar to claim 1. For reasons similar to those discussed above with respect to claim 1, withdrawal of the rejection and allowance of claim 14 are respectfully requested.

Claims 18 and 20 are dependent on claim 14 and are believed to be allowable for at least the reasons claim 14 is allowable. Accordingly, withdrawal of the rejection and allowance of claims 18 and 20 are respectfully requested.

Claims 4, 6, 9, 17 and 19 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fried. The rejection is respectfully traversed.

The Office Action admits that Fried does not disclose or suggest the features of claims 4, 6, 9, 17 and 19, but states that it would have been obvious to have the width of the oxide layer, the first and second spacers and the fin structure within the claimed ranges "since it has been held that where the general condition of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art" and relies upon In re Aller for support (Office Action – page 4). The applicants respectfully disagree.

The mere statement that the claimed ranges recited in claims 4, 6, 9, 17 and 19 involves only routine skill in the art and therefore would be obvious is not supported by the disclosure of Fried and does not satisfy the requirements of 35 U.S.C. § 103. For example, Fried is totally silent with respect to the widths of any of the structures in Fried. The applicants, therefore, assert that Fried cannot be fairly construed to suggest the width of oxide layer 110 in Fried ranges from about 10Å to about 100 Å, as required by claims 4 and 19, the width of the first and second spacers 115 in Fried ranges from about 100 Å to about 500 Å, as required by claims 6

and 17 or the width of the fin stack 105 in Fried ranges from about 100 Å to about 1000 Å, as required by claim 9.

Per se rules regarding obviousness, such as that allegedly established by the Aller case, do not exist and therefore reliance on such rules to establish obviousness under 35 U.S.C. §103(a) is improper. See In re Ochiai, 71 F.3d 1565, 1570, 37 USPQ2d 1127, 1132 (Fed. Cir. 1995); In re Wright, 343 F.2d 761, 769-70, 145 USPQ 182, 190 (CCPA 1965). The applicants, therefore, respectfully request that any subsequent communication point to some objective motivation or suggestion as to why it would have been obvious to form the structures in Fried to read on the features recited in claims 4, 6, 9, 17 and 19 or withdraw the rejection.

For at least these additional reasons, withdrawal of the rejection and allowance of claims 4, 6, 9, 17 and 19 are respectfully requested.

NEW CLAIMS

New claims 21 and 22 have been added. These claims are believed to be allowable over the cited art. For example, claim 21 recites features similar to those discussed above with respect to claims 1, 2, 4 and 6. The cited art does not disclose or suggest these features. Claim 22 is dependent on claim 21 and is believed to be allowable for at least the reasons claim 21 is allowable. In addition, claim 22 recites that the gate dielectric comprises an oxide having a thickness ranging from about 50 Å to about 200 Å. The cited references do not disclose or suggest this feature. Accordingly, allowance of claims 21 and 22 is respectfully requested.

**CONCLUSION**

In view of the foregoing amendments and remarks, the applicants respectfully request withdrawal of the outstanding rejections and the timely allowance of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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